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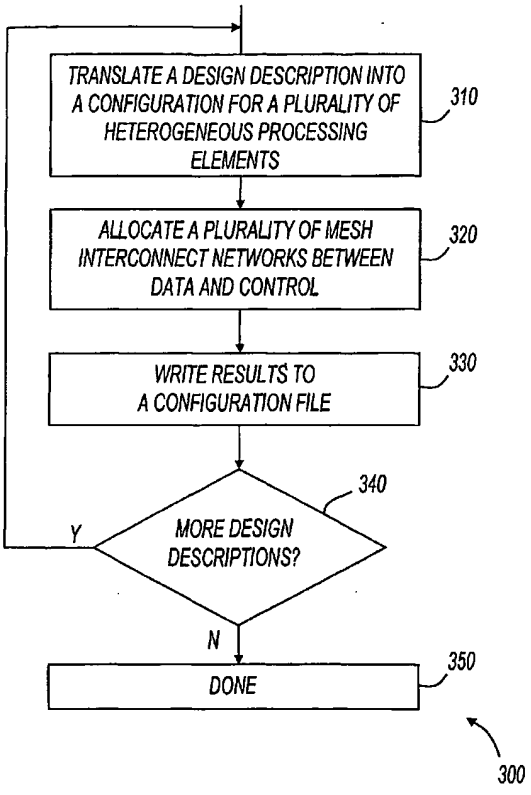
(54) Title: ALLOCATION OF COMBINED OR SEPARATED DATA AND CONTROL MESH INTERCONNECT NETWORKS



(57) Abstract: A dual mesh interconnect network in a heterogeneous configurable circuit may be allocated between data communication and control communication.

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ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ALBANESI M G ET AL: "A VLSI 128-processor chip for multiresolution image processing" MASSIVELY PARALLEL COMPUTING SYSTEMS, 1994., PROCEEDINGS OF THE FIRST INTERNATIONAL CONFERENCE ON ISCHIA, ITALY 2-6 MAY 1994, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, 2 May 1994 (1994-05-02), pages 296-307, XP010125887 ISBN: 0-8186-6322-7	1,2,5-7, 9-11,14, 15,17, 21-23, 27,28
Y	abstract page 296 - page 299 figures 2,4	3,4,12, 18-20, 24-26, 29,30

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
16 September 2005	07/10/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Alonso Nogueiro, L

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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HUI ZHANG ET AL: "Interconnect architecture exploration for low-energy reconfigurable single-chip DSPs" VLSI '99. PROCEEDINGS. IEEE COMPUTER SOCIETY WORKSHOP ON ORLANDO, FL, USA 8-9 APRIL 1999, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 8 April 1999 (1999-04-08), pages 2-8, XP010330307 ISBN: 0-7695-0152-4	1,2,5-7, 9-11,14, 15,17, 21-23, 27,28
A	abstract page 2 - page 7 figures 1,7,9,11	3,4,12, 18-20, 24-26, 29,30
Y	MARESCAUX T ET AL: "Networks on chip as hardware components of an OS for reconfigurable systems" FIELD-PROGRAMMABLE LOGIC AND APPLICATIONS. 13TH INTERNATIONAL CONFERENCE, FPL 2003. PROCEEDINGS (LECTURE NOTES IN COMPUT. SCI. VOL.2778) SPRINGER-VERLAG BERLIN, GERMANY, 2003, pages 595-605, XP002345294 ISBN: 3-540-40822-3 page 595 - page 596 page 598 - page 603	3,4,12, 18-20, 24-26, 29,30
A	US 6 226 735 B1 (MIRSKY ETHAN A) 1 May 2001 (2001-05-01) column 10 - column 11 figures 15-18	3,4,12, 18-20, 24-26, 29,30

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6226735 B1	01-05-2001	US 2001029515 A1	11-10-2001